FIG. 1
PRIOR ART

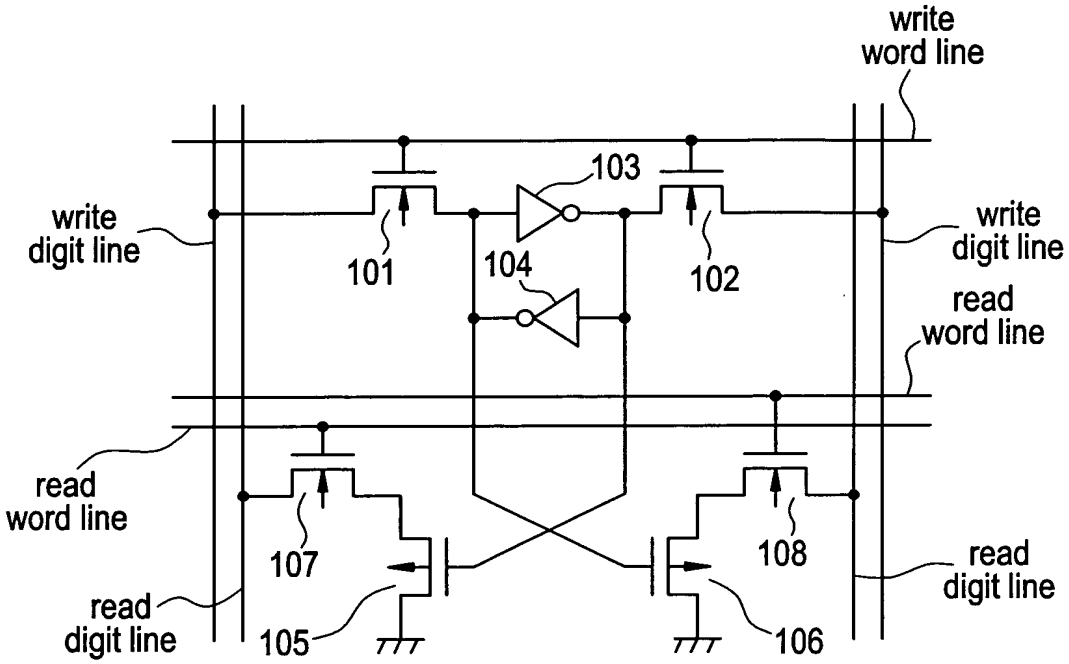


FIG. 2
PRIOR ART

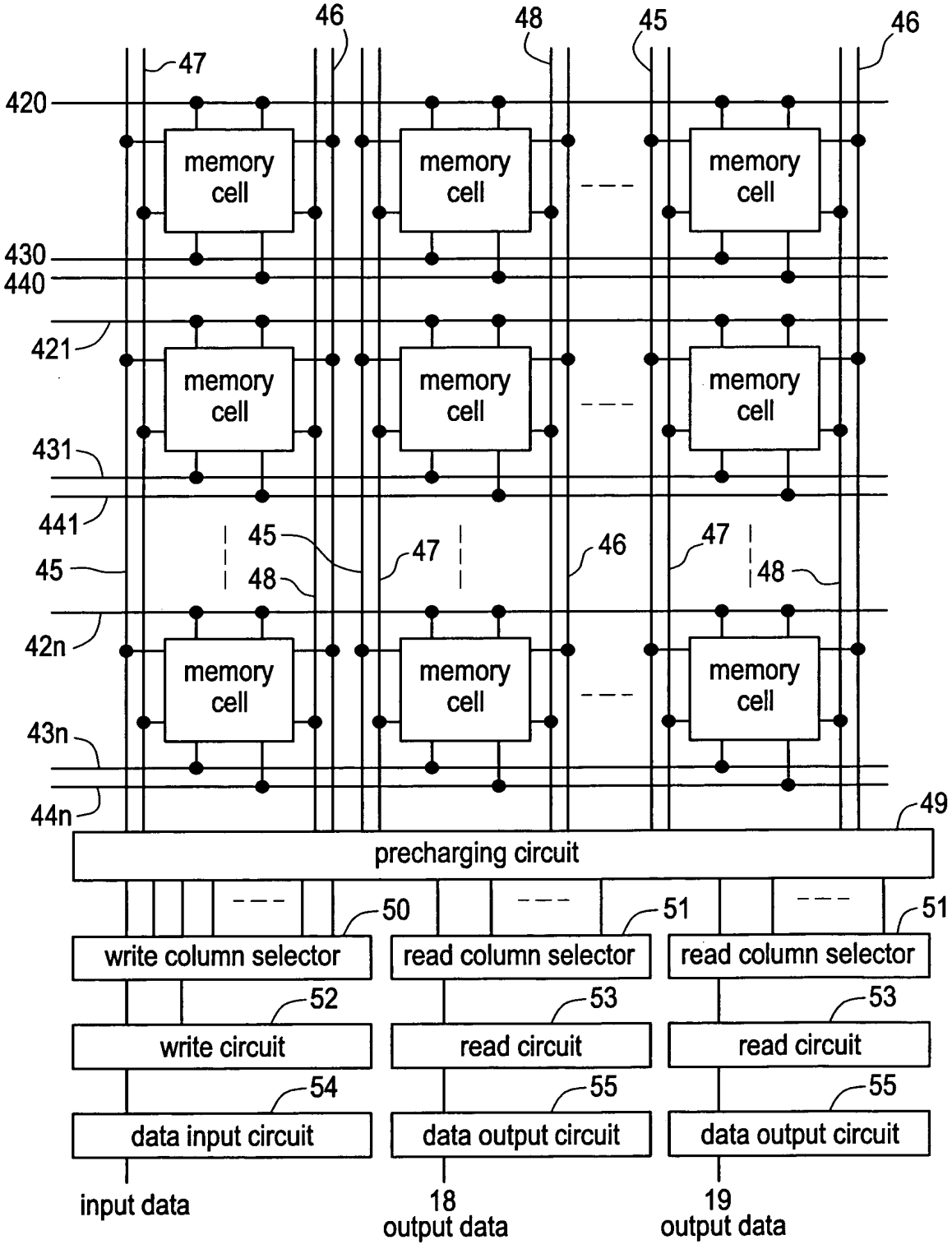


FIG. 3
PRIOR ART

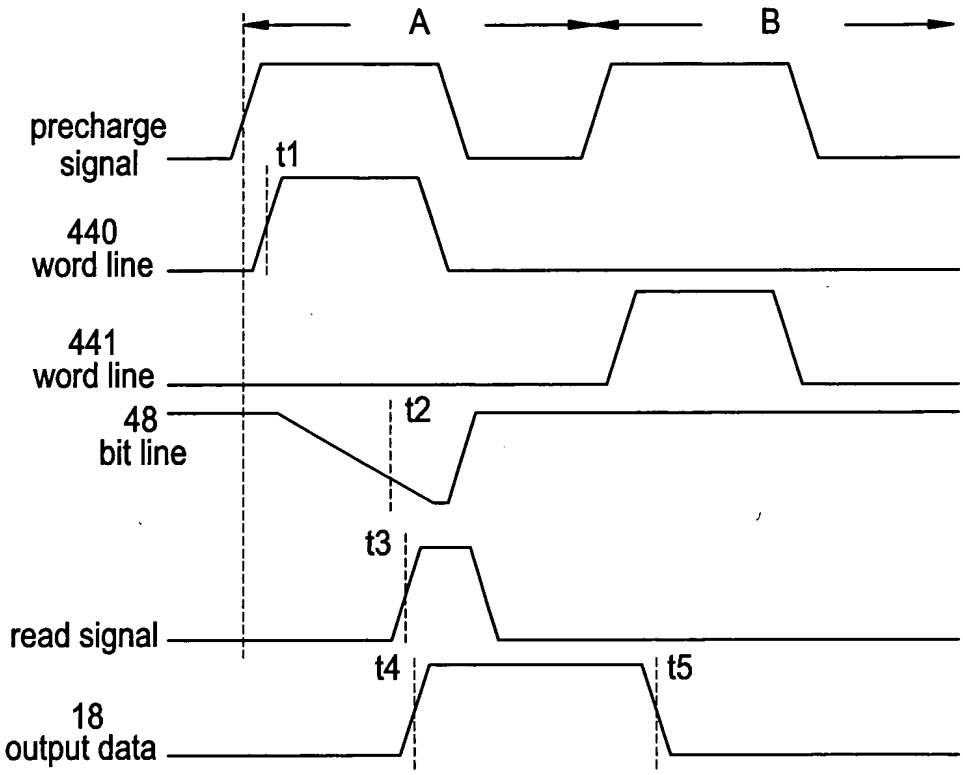


FIG. 4

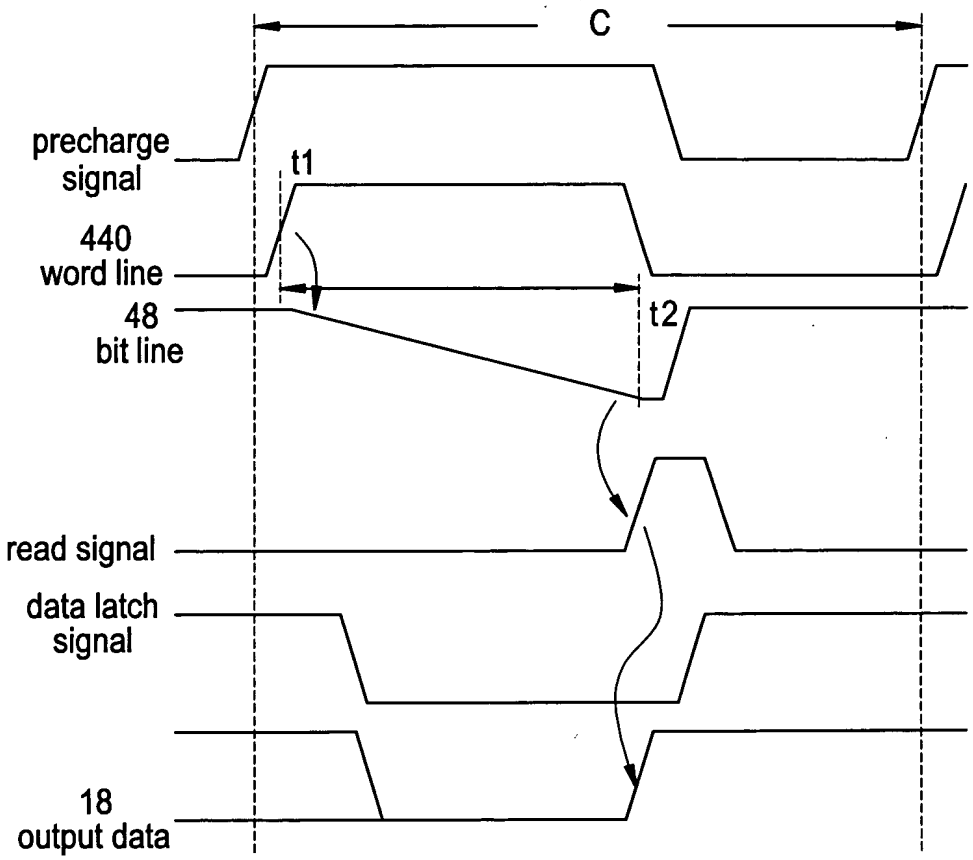

C
precharge signal
t1
440 word line
48 bit line
t2
read signal
data latch signal
18 output data

FIG. 5
PRIOR ART

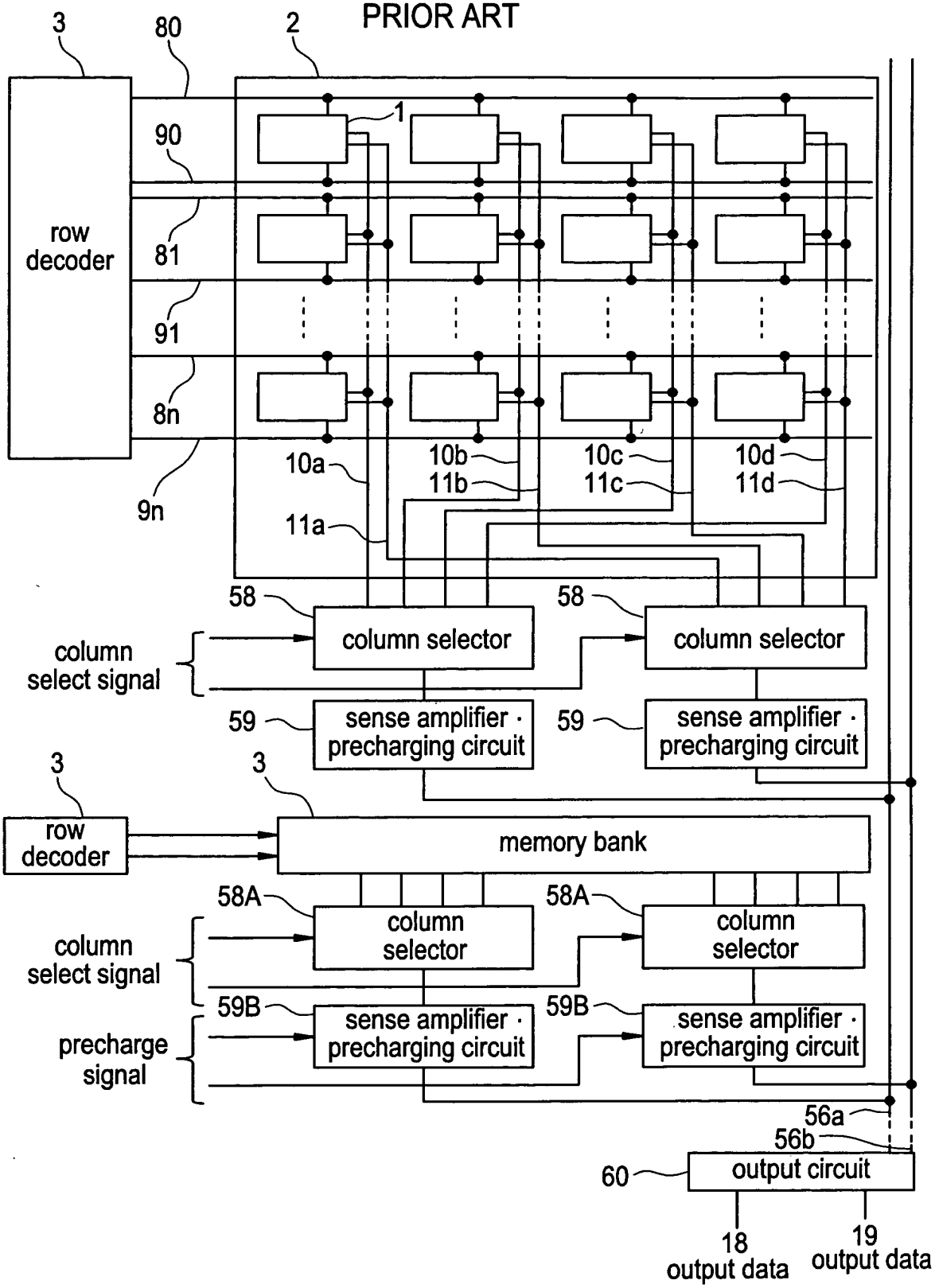


FIG. 6
PRIOR ART

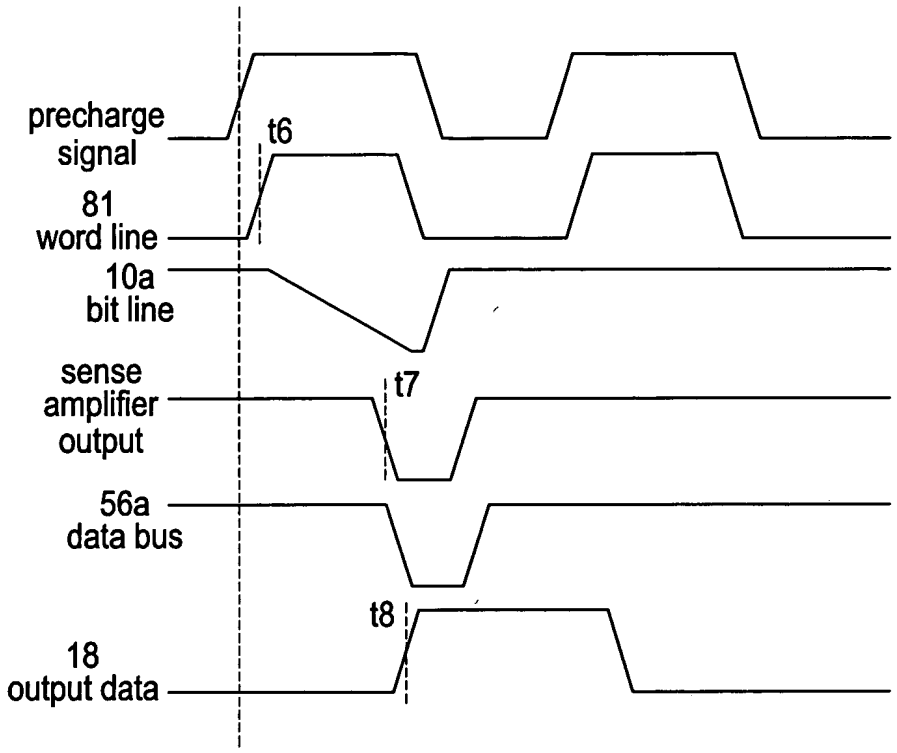


FIG. 7
PRIOR ART

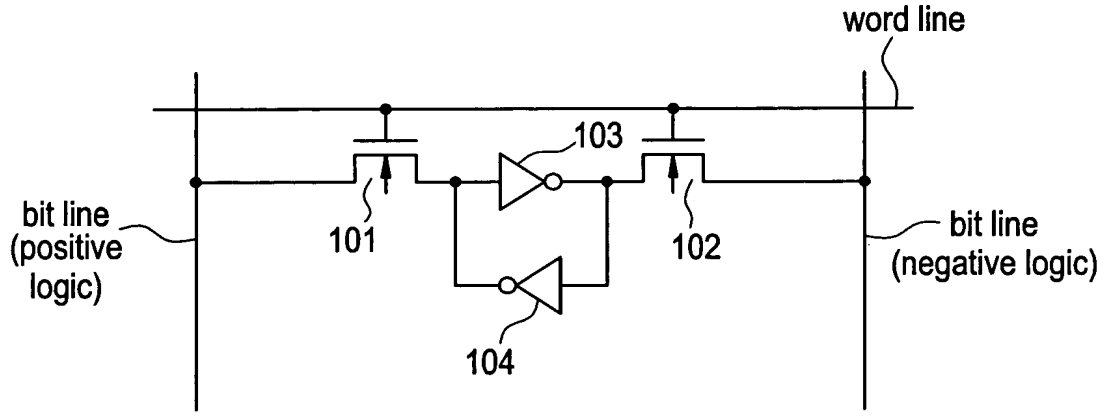


FIG. 8

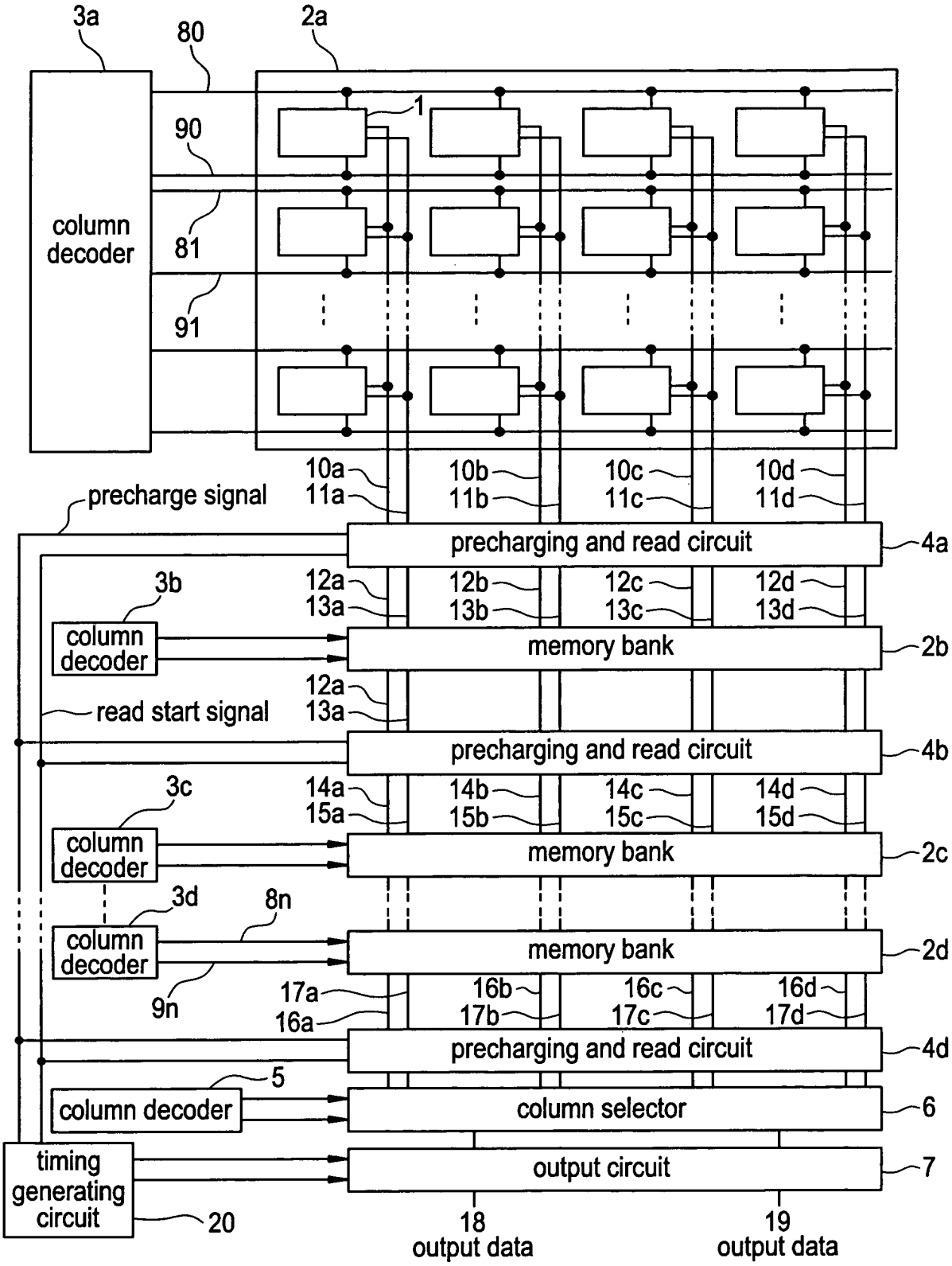

3a
80
2a
1
90
column decoder
81
91
10a
11a
10b
11b
10c
11c
10d
11d
precharge signal
precharging and read circuit
4a
3b
12a
13a
12b
13b
12c
13c
12d
13d
column decoder
memory bank
2b
read start signal
12a
13a
precharging and read circuit
4b
3c
14a
15a
14b
15b
14c
15c
14d
15d
column decoder
memory bank
2c
3d
8n
column decoder
memory bank
2d
9n
17a
16a
16b
17b
16c
17c
16d
17d
precharging and read circuit
4d
5
column decoder
column selector
6
timing generating circuit
20
output circuit
7
18
output data
19
output data

FIG. 9

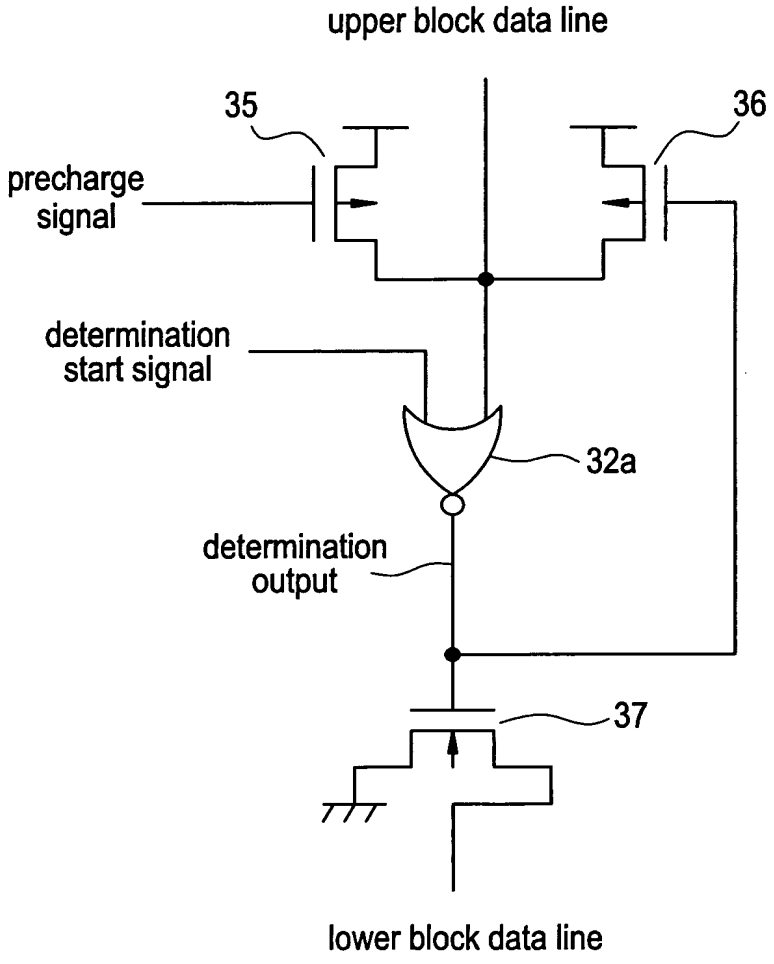

upper block data line
35
36
precharge signal
determination start signal
32a
determination output
37
lower block data line

FIG. 10

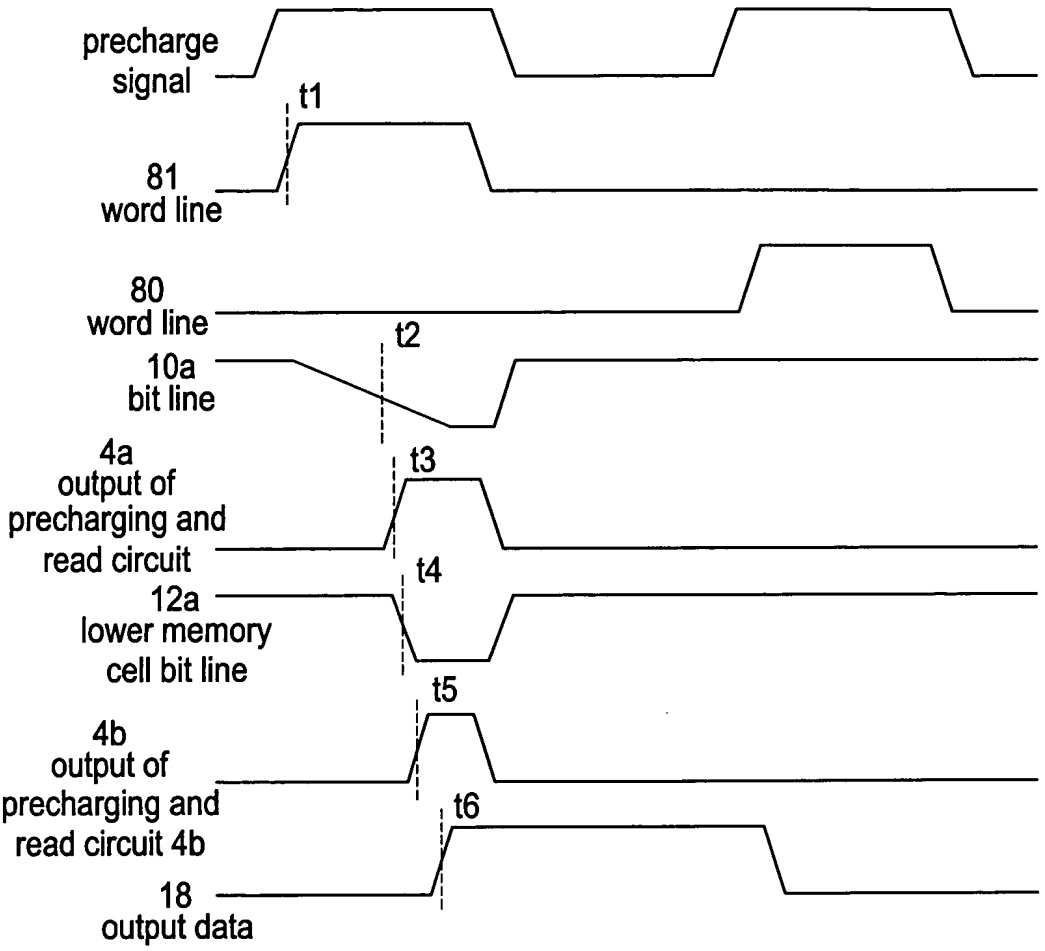

precharge signal
t1
81 word line
80 word line
t2
10a bit line
4a output of precharging and read circuit
t3
t4
12a lower memory cell bit line
t5
4b output of precharging and read circuit 4b
t6
18 output data

FIG. 11

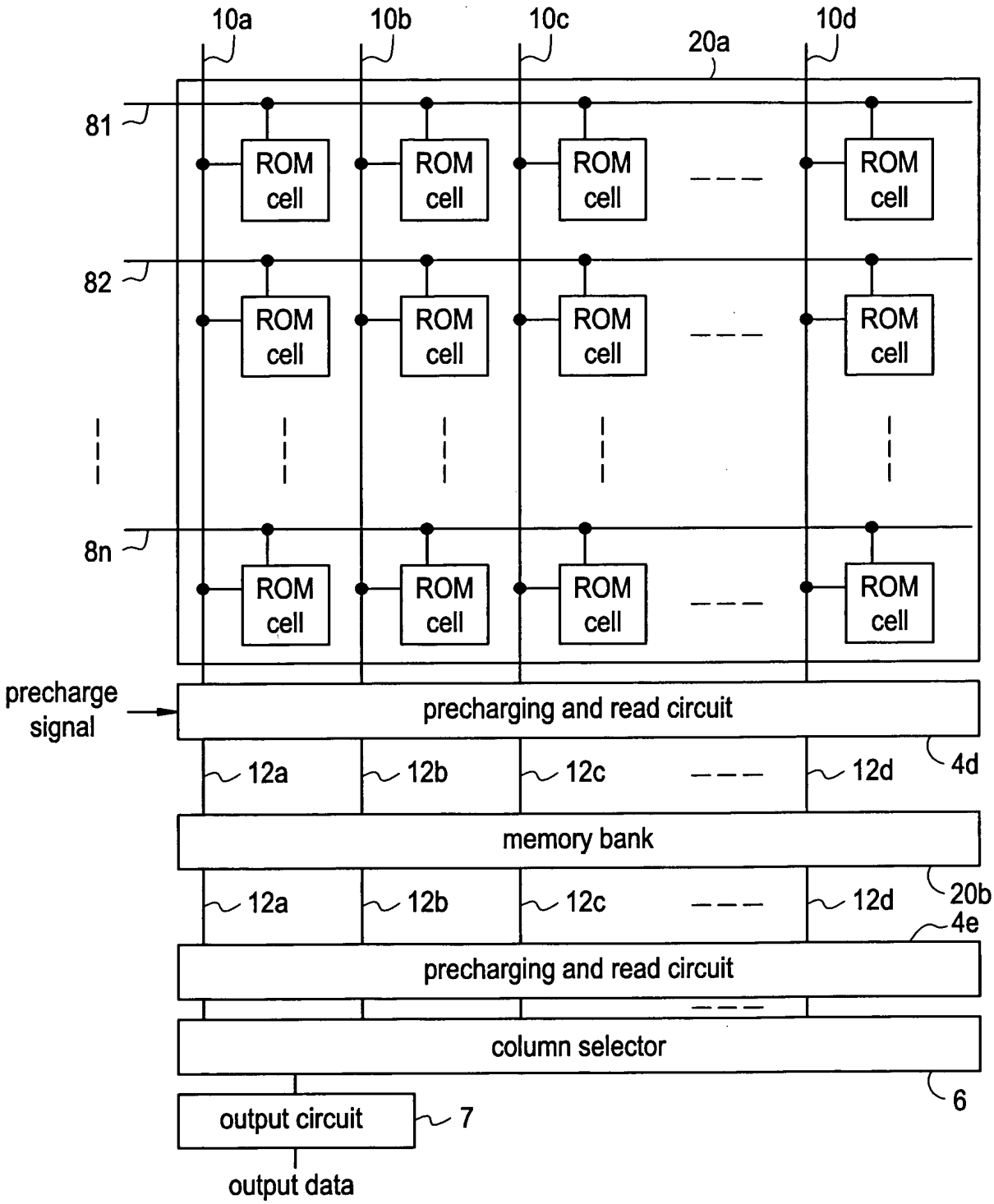

10a
10b
10c
20a
10d
81
82
8n
ROM cell
precharge signal
precharging and read circuit
4d
12a
12b
12c
12d
memory bank
20b
4e
column selector
6
output circuit
7
output data

FIG. 12

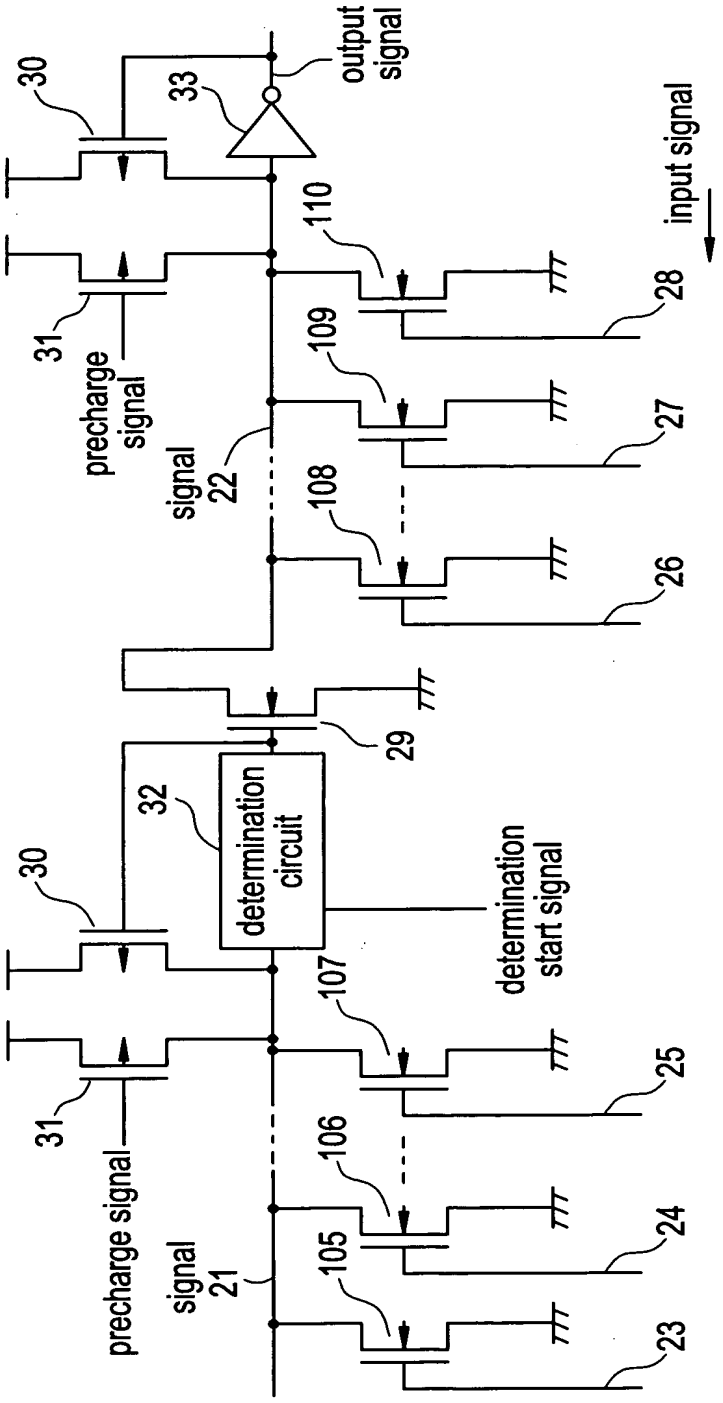

output signal
input signal
30
33
110
31
precharge signal
109
28
27
signal 22
108
26
29
32
determination circuit
determination start signal
30
107
31
precharge signal
106
25
24
signal 21
105
23

FIG. 13

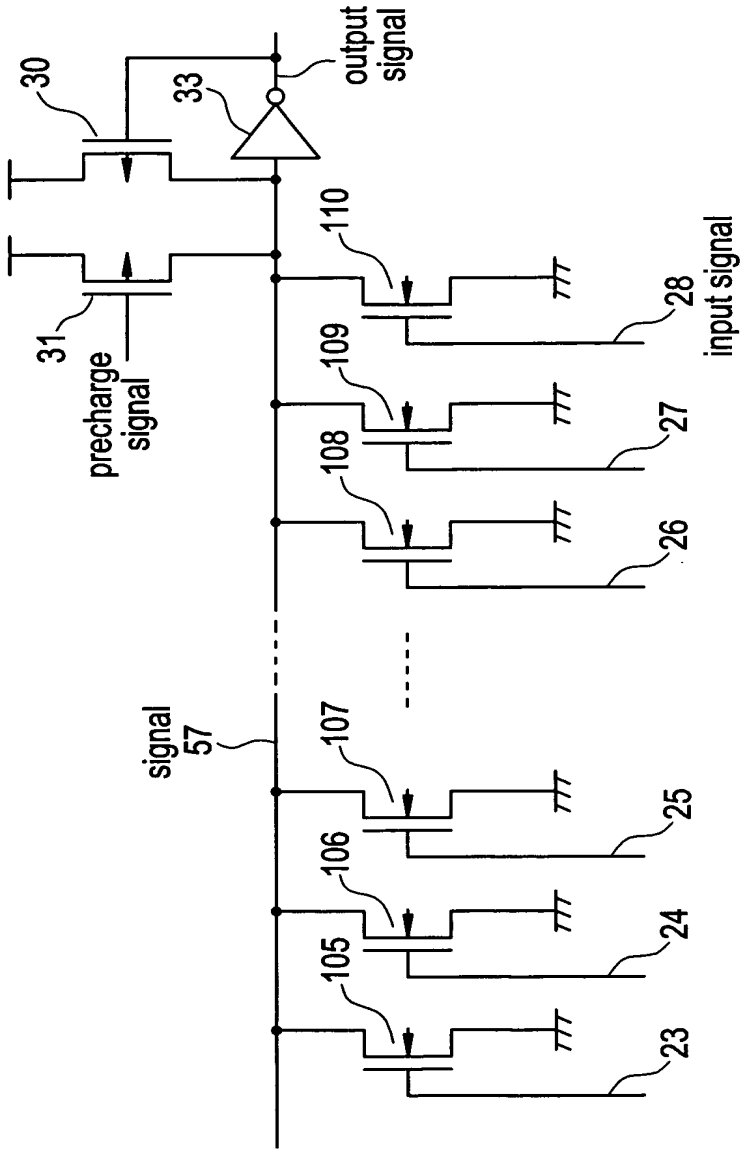

30
33
output signal
110
28
input signal
31
precharge signal
109
27
108
26
signal 57
107
25
106
24
105
23

FIG. 14

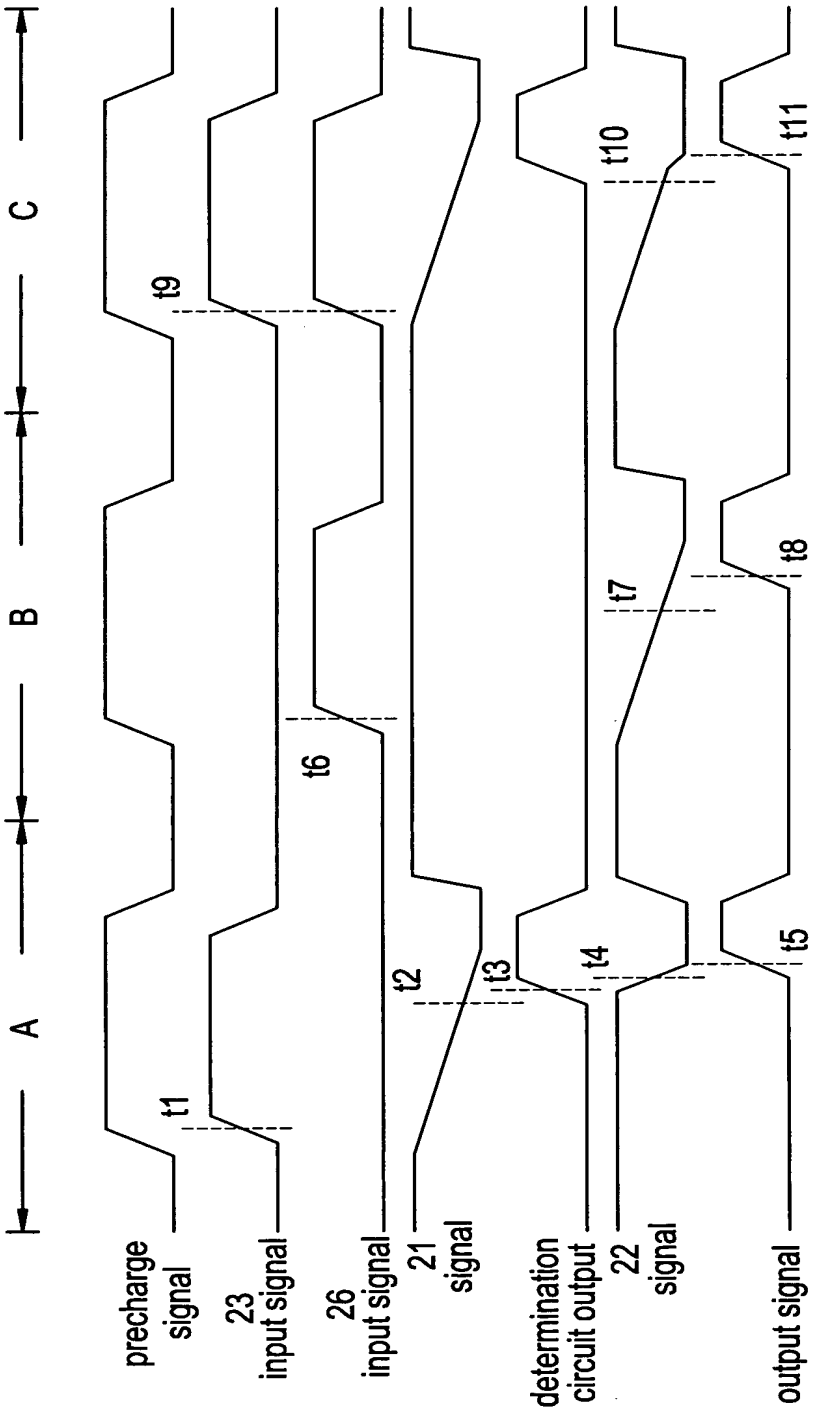

A
B
C
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
precharge signal
23 input signal
26 input signal
21 signal
determination circuit output
22 signal
output signal

FIG. 15

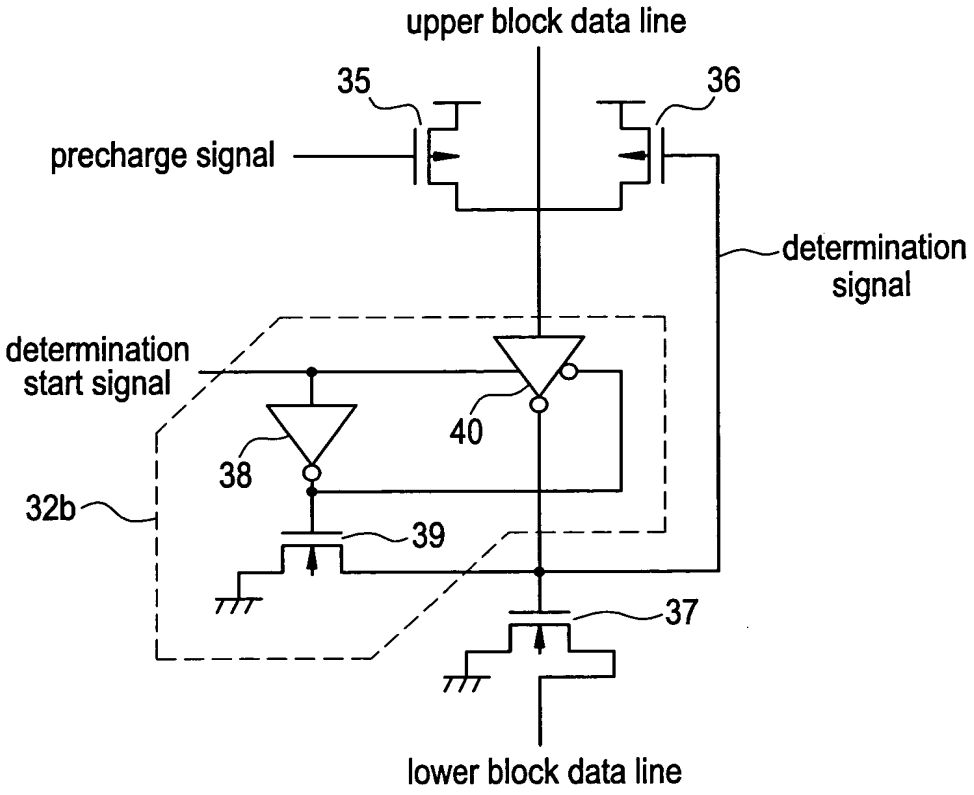
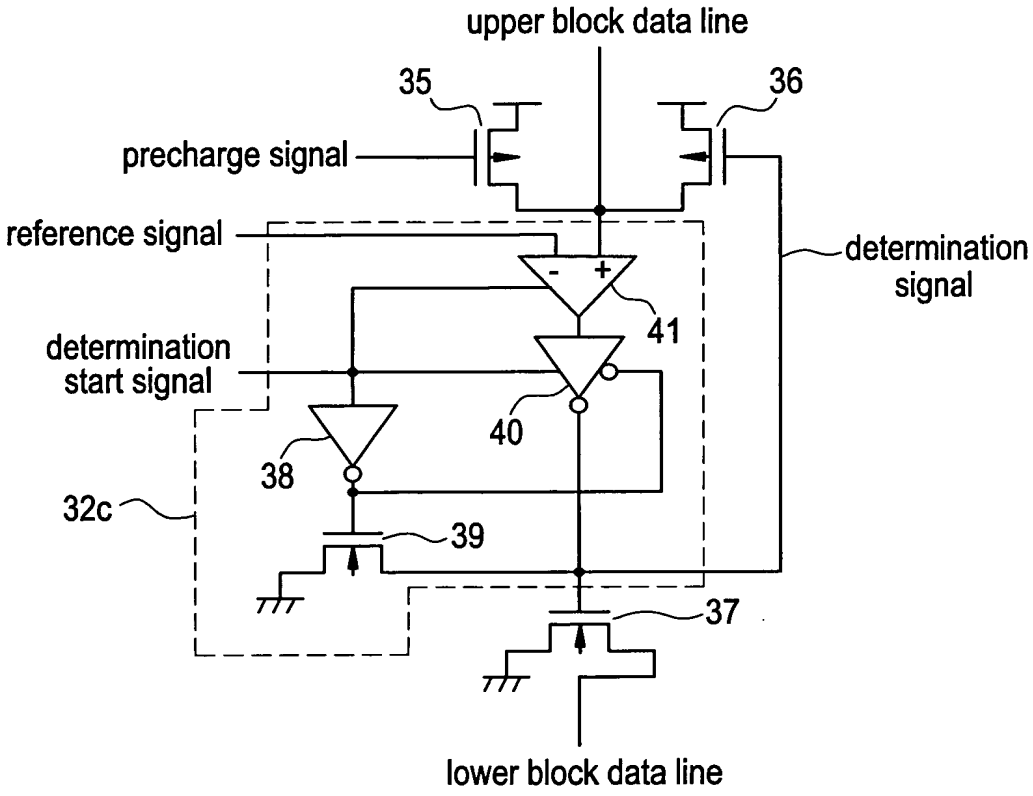

upper block data line
35
36
precharge signal
determination signal
determination start signal
40
38
32b
39
37
lower block data line

FIG. 16


upper block data line
35
36
precharge signal
reference signal
determination signal
-
+
41
determination start signal
40
38
32c
39
37
lower block data line